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PCI Express 1:8 HCSL Clock Buffer

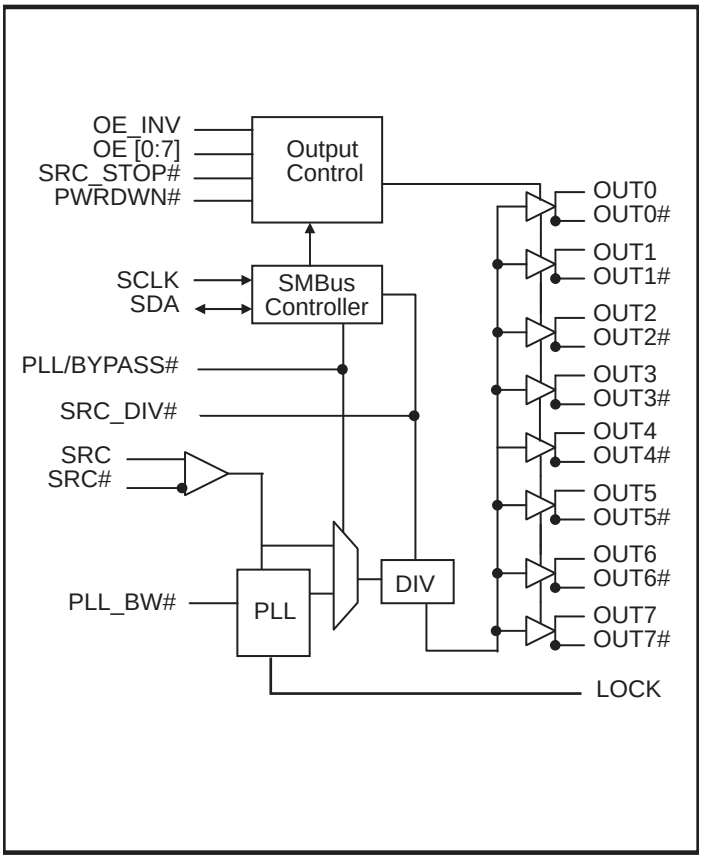
Features

- Phase jitter filter for PCIe application
- Eight Pairs of Differential Clocks
- Low skew < 50ps
- Low Cycle-to-cycle jitter < 50ps
- Output Enable for all outputs
- Outputs Tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or Fanout operation
- 3.3V Operation
- Packaging (Pb-Free & Green):
  — 48-Pin SSOP (V)
  — 48-Pin TSSOP (A)

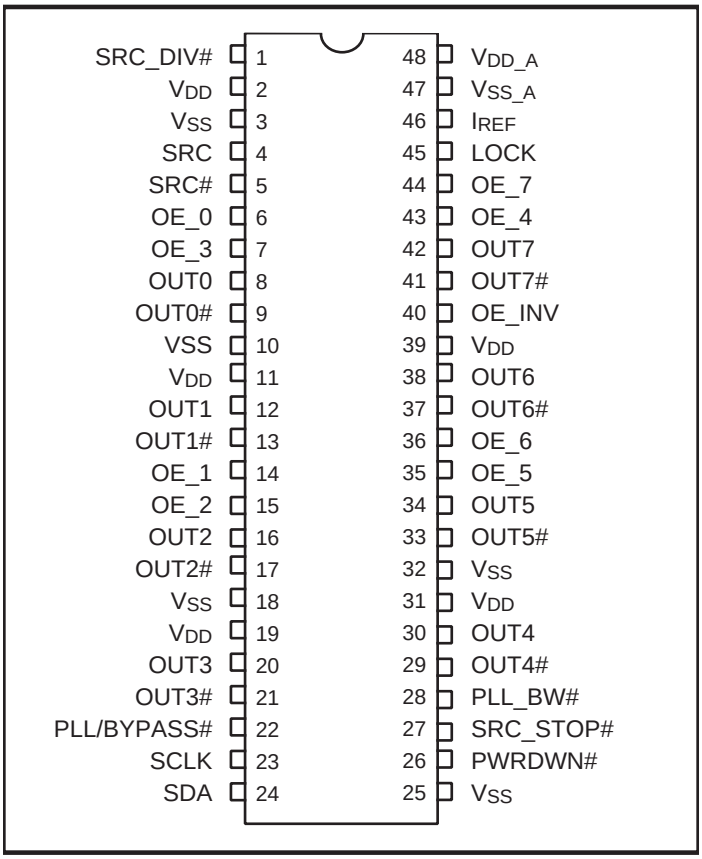
Description

PI6C20800S is a PCI Express, high-speed, low-noise differential clock buffer designed to be a companion to PI6C410BS PCI Express clock generator for Intel server chipsets. The device distributes the differential SRC clock from PI6C410BS to eight differential pairs of clock outputs either with or without PLL. The input SRC clock can be divided by 2 when SRC_DIV# is LOW. The clock outputs are controlled by input selection of SRC_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC_STOP# or PWRDWN# is LOW, the output clocks are Tristated. When PWRDWN# is LOW, the SDA and SCLK inputs must be Tristated.

Block Diagram



Pin Configuration



Pin Descriptions

Pin Name	Type	Pin #	Descriptions
SRC_DIV#	Input	1	3.3V LVTTL input for selecting input frequency divide by 2, active LOW.
SRC & SRC#	Input	4, 5	0.7V Differential SRC input from PI6C410 clock synthesizer
OE [0:7]	Input	6, 7, 14, 15, 35, 36, 43, 44	3.3V LVTTL input for enabling outputs, active HIGH.
OE_INV	Input	40	3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE[0:7], SRC_STOP#, PWRDWN# inverted.
OUT[0:7] & OUT[0:7]#	Output	8, 9, 12, 13, 16 17, 20, 21, 29, 30, 33, 34, 37, 38, 41, 42	0.7V Differential outputs
PLL/BYPASS#	Input	22	3.3V LVTTL input for selecting fan-out of PLL operation.
SCLK	Input	23	SMBus compatible SCLOCK input
SDA	I/O	24	SMBus compatible SDATA
I_{REF}	Input	46	External resistor connection to set the differential output current
SRC_STOP#	Input	27	3.3V LVTTL input for SRC stop, active LOW
PLL_BW#	Input	28	3.3V LVTTL input for selecting the PLL bandwidth
PWRDWN#	Input	26	3.3V LVTTL input for Power Down operation, active LOW
LOCK	Output	45	3.3V LVTTL output, transition high when PLL lock is achieved (Latched output)
V_{DD}	Power	2, 11, 19, 31, 39	3.3V Power Supply for Outputs
V_{SS}	Ground	3, 10, 18, 25, 32	Ground for Outputs
V_{SS_A}	Ground	47	Ground for PLL
V_{DD_A}	Power	48	3.3V Power Supply for PLL

Serial Data Interface (SMBus)

PI6C20800S is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	1	1	0	0/1

Data Protocol(1)

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1	8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	SRC_DIV# 0 = Divide by 2 1 = Normal	RW	1 = x1	OUT[0:7], OUT[0:7]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:7], OUT[0:7]#	NA
2	PLL Bandwidth 0 = HIGH Bandwidth, 1 = LOW Bandwidth	RW	1 = Low	OUT[0:7], OUT[0:7]#	NA
3	RESERVED				
4	RESERVED				
5	RESERVED				
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	NA

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	OUTPUTS enable 1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT0, OUT0#	NA
1		RW	1 = Enabled	OUT1, OUT1#	NA
2		RW	1 = Enabled	OUT2, OUT2#	NA
3		RW	1 = Enabled	OUT3, OUT3#	NA
4		RW	1 = Enabled	OUT4, OUT4#	NA
5		RW	1 = Enabled	OUT5, OUT5#	NA
6		RW	1 = Enabled	OUT6, OUT6#	NA
7		RW	1 = Enabled	OUT7, OUT7#	NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT0, OUT0#	NA
1		RW	0 = Free running	OUT1, OUT1#	NA
2		RW	0 = Free running	OUT2, OUT2#	NA
3		RW	0 = Free running	OUT3, OUT3#	NA
4		RW	0 = Free running	OUT4, OUT4#	NA
5		RW	0 = Free running	OUT5, OUT5#	NA
6		RW	0 = Free running	OUT6, OUT6#	NA
7		RW	0 = Free running	OUT7, OUT7#	NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	RESERVED	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

Data Byte 4: Pericom ID Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

Functionality

PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	I_{REF} × 2 or Float	LOW	0	I_{REF} × 6 or Float	LOW

Power Down (PWRDWN# assertion)

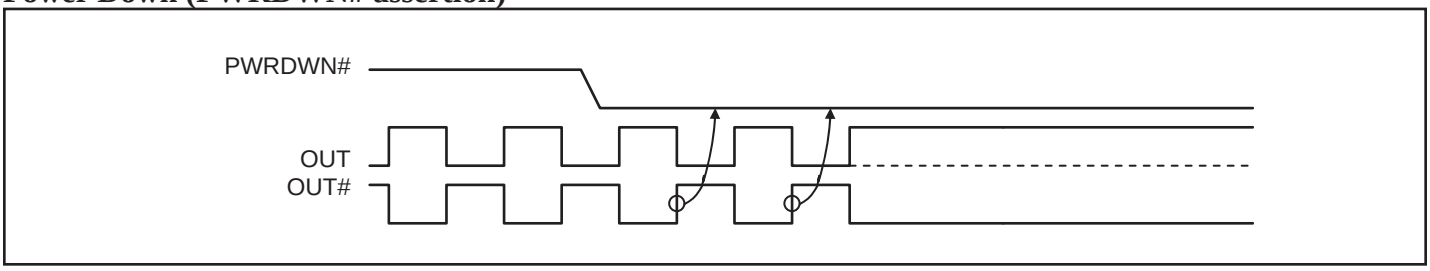


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

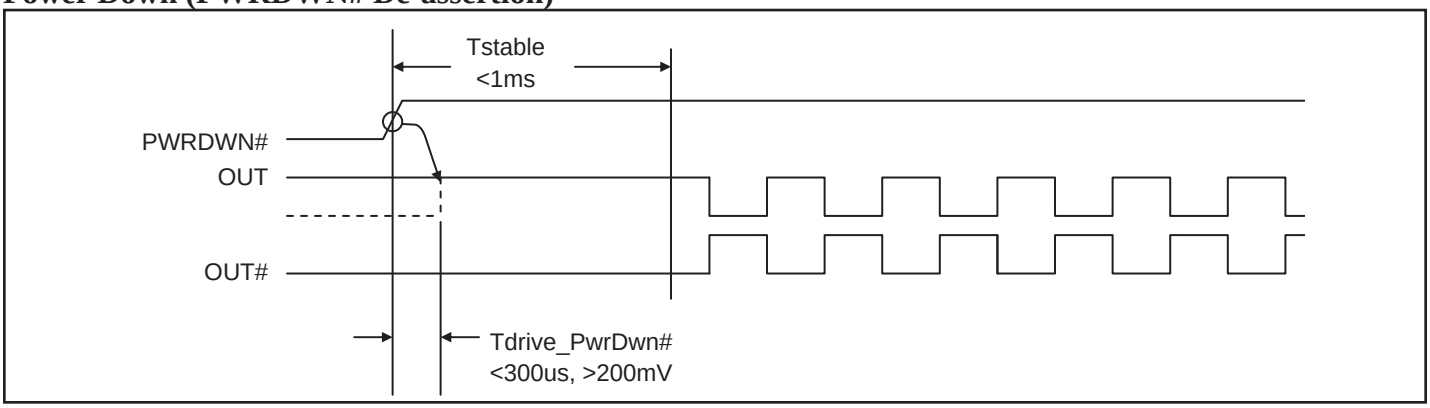


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:7], OUT[0:7]#

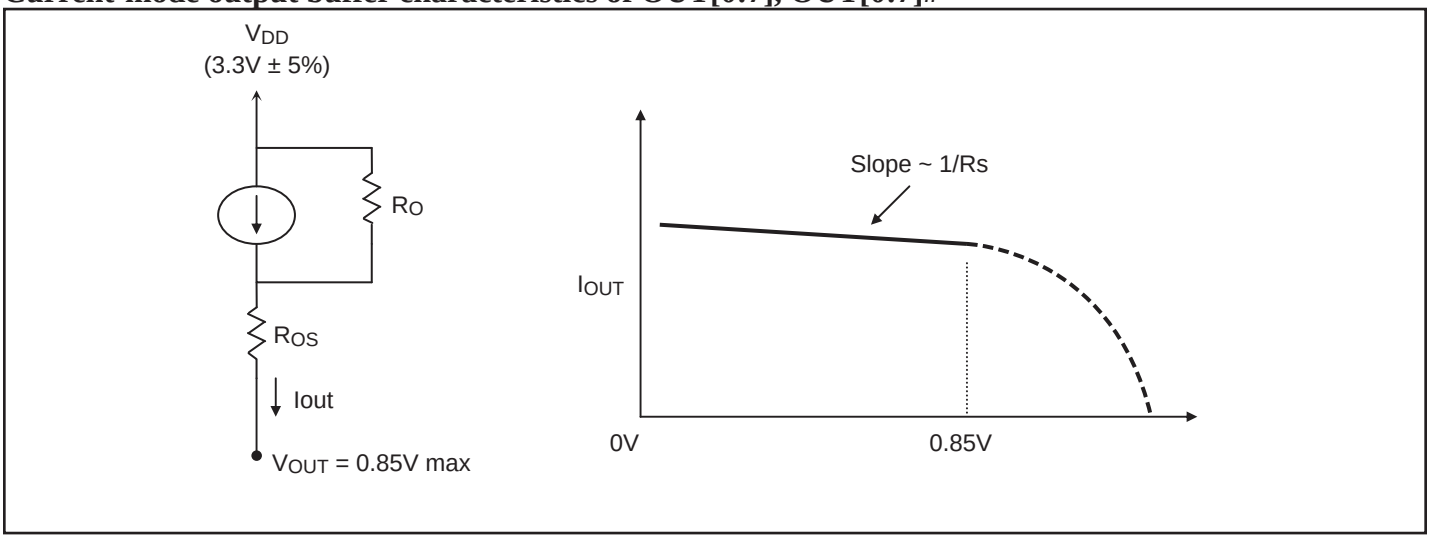


Figure 9. Simplified diagram of current-mode output buffer

Differential Clock Buffer characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	V_{DD} = 3.30 ±5%	R_{REF} = 475Ω 1% I_{REF} = 2.32mA	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note:
1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3xRr)	Output Current	V_{OH} @ Z
100Ω (100Ω differential ≈ 15% coupling ratio)	R_{REF} = 475Ω 1%, I_{REF} = 2.32mA	I_{OH} = 6 x I_{REF}	0.7V @ 50

Absolute Maximum Ratings(1) (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input HIGH Voltage		4.6	
V_{IL}	Input LOW Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

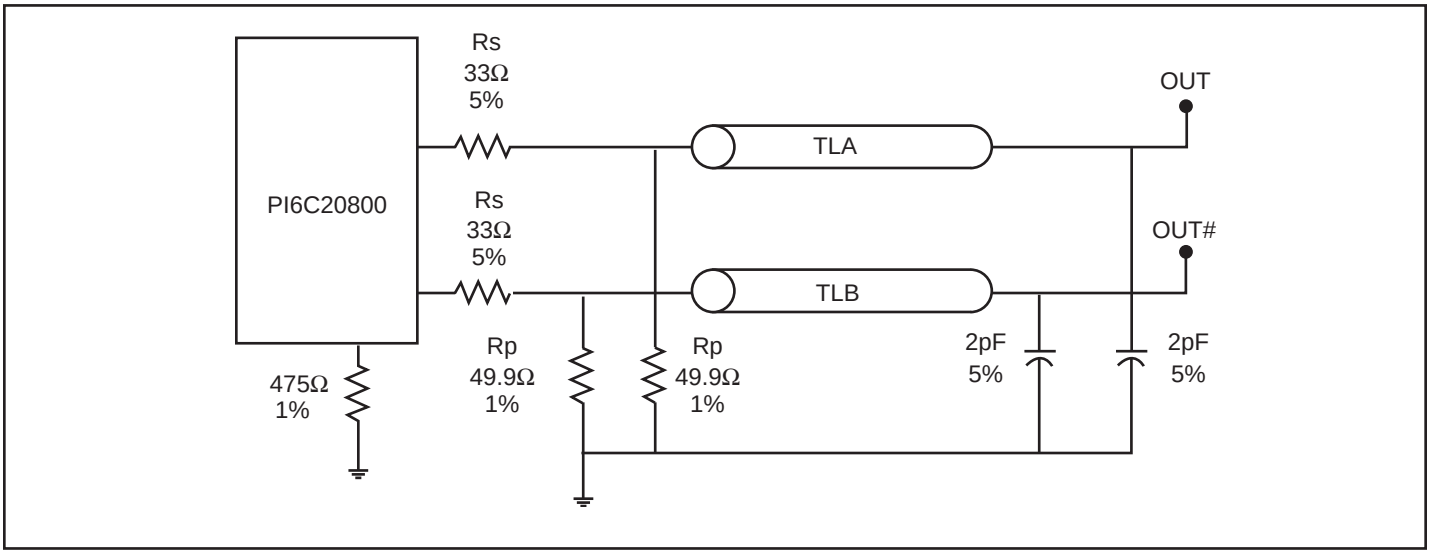
Symbol	Parameters	Condition	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V_{IH}	3.3V Input HIGH Voltage	V_{DD}	2.0	V_{DD} + 0.3	
V_{IL}	3.3V Input LOW Voltage		V_{SS} – 0.3	0.8	
I_{IK}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	µA
V_{OH}	3.3V Output HIGH Voltage	I_{OH} = -1mA	2.4		V
V_{OL}	3.3V Output LOW Voltage	I_{OL} = 1mA		0.4	
I_{OH}	Output HIGH Current	I_{OH} = 6 x I_{REF}, I_{REF} = 2.32mA	12.2		mA
				15.6	
C_{IN}	Logic Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	
L_{PIN}	Pin Inductance			7	nH
I_{DD}	Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 100MHz		250	mA
I_{SS}	Power Down Current	Driven outputs		80	
I_{SS}	Power Down Current	Tristate outputs		12	
T_A	Ambient Temperature		0	70	°C

AC Switching Characteristics[1,2,3] (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

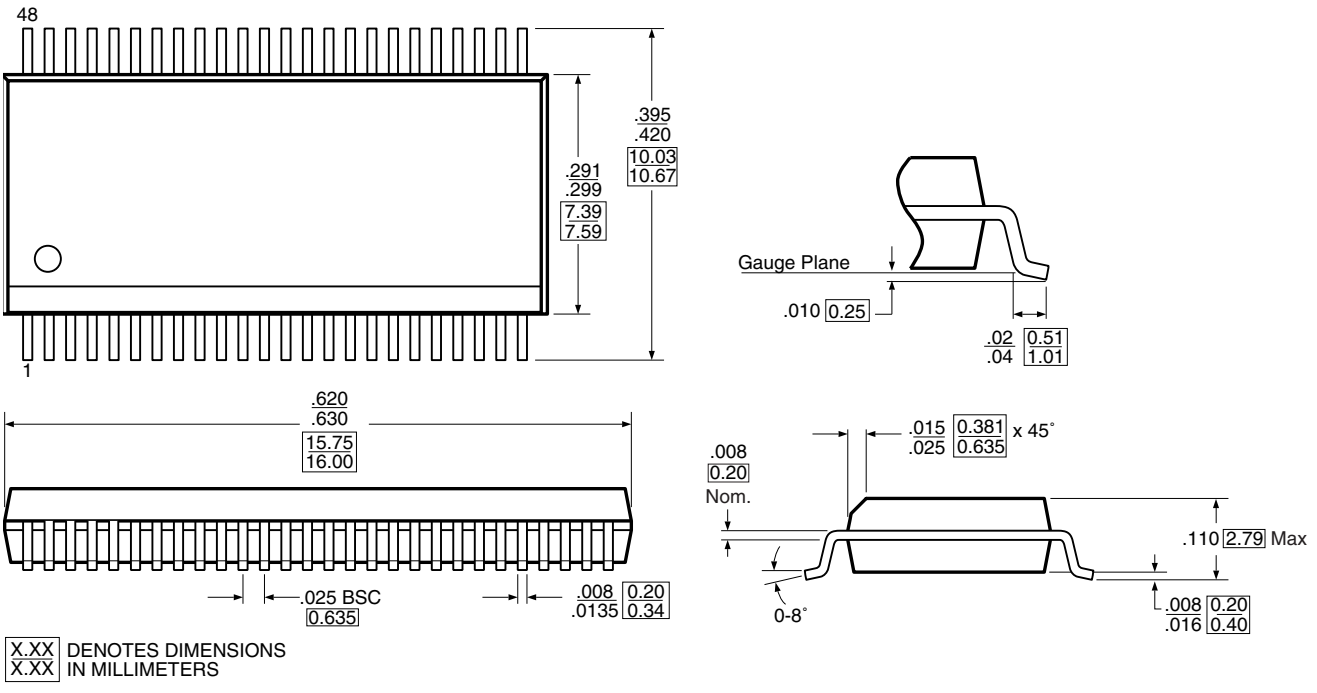
Symbol	Parameters		Min	Max.	Units	Notes
F_{in}	SRC/SRC# Input Frequency PLL Mode			100	MHz	6
	SRC/SRC# Input Frequency Bypass Mode		100	400	MHz	6
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)		175	700	ps	2
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation			125		2
T_{pd}	Input to Output Propagation Delay	PLL Mode	-250	250	ps	
		Bypass Mode	2.5	6.5	ns	
T_{skew}	Output-to-Output Skew			50	ps	3
V_{HIGH}	Voltage HIGH (Measured at 100MHz @ 3.3V)		660	850	mV	2
V_{OVS}	Max. Voltage			1150		
V_{UDS}	Min. Voltage		-300			
V_{LOW}	Voltage LOW		-150	+150		2
V_{cross}	Absolute crossing poing voltages		250	550		2
ΔV_{cross}	Total Variation of V_{cross} over all edges			140		2
T_{DC}	Duty Cycle (Measured at 100 MHz)		45	55	%	3
$T_{jcyc-cyc}$	Jitter, Cycle-to-cycle (PLL Mode, Measurement for differential waveform)			50	ps	4
	Jitter, Cycle-to-cycle (BYPASS mode as additive jitter)					
J_{add}	Additive RMS phase jitter for PCIe GenII		<0	1	ps	5

Notes:
1. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measured using M1 timing analyzer from Amherst.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe Gen II filter. ($J_{add} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)
6. –0.5% downnspread input

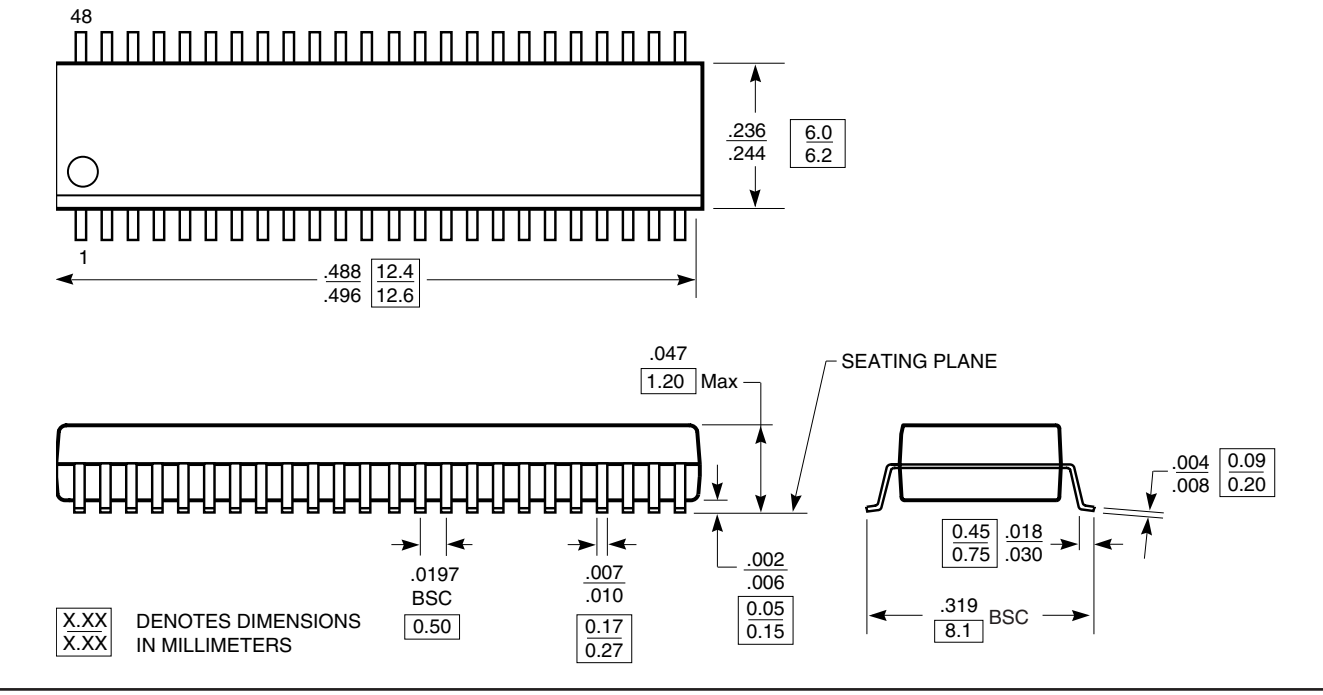
Configuration Test Load Board Termination



Packaging Mechanical: 48-Pin SSOP (V)



Packaging Mechanical: 48-Pin TSSOP (A)



Ordering Information(1,2)

Ordering Code	Package Code	Package Description
PI6C20800SVE	VE	48-pin, 300-mil wide, SSOP, Pb-Free and Green
PI6C20800SAE	AE	48-pin, 240-mil wide, TSSOP, Pb-Free and Green

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green